Please amend the application as follows:

IN THE CLAIMS:

Claims 1-16 (Canceled)

17. (Currently Amended) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space, wherein overmolding produces a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across a length of the encapsulant.

18. (Canceled)

19. (Canceled)

20. (Original) The method of claim 17 further comprising the step of singulating the plurality of package sites after overmolding.

21. (Original) The method of claim 20 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

22. (Original) The method of claim 21 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

23. (New) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in at least a four by four array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each site; and

overmolding a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space to produce a top surface of the encapsulant which has a surface deviation of less than 0.13 millimeters across the top surface of the encapsulant.

24. (New) The method of claim 23 further comprising the step of singulating the plurality of package sites after overmolding.

25. (New) The method of claim 24 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

26. (New) The method of claim 25 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.

27. (New) A method for making a packaged semiconductor device comprising:

providing an interconnect substrate having a plurality of substantially identical package sites arranged in an array, the plurality of sites being separated by a singulation space;

mounting and interconnecting a semiconductor device within each package site; and

overmolding an encapsulant over the plurality of sites and the singulation space to have a top surface planarity deviation of less than 0.13 millimeters.

28. (New) The method of claim 27 further comprising the step of singulating the plurality of package sites after overmolding.

29. (New) The method of claim 28 wherein singulating comprises sawing through the single and continuous encapsulant and the interconnect substrate along the singulation space.

30. (New) The method of claim 29 wherein singulating produces a plurality of packaged semiconductor devices, and further comprising the step of handling each packaged semiconductor device with automated pick and place equipment.